AN INVESTIGATION OF THE EFFECTS OF EMITTER PRE-DEPOSITION TEMPERATURE IN DOUBLE-DIFFUSED POLYSILICON EMITTER BIPOLAR TRANSISTORS

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ABSTRACT

The effects of emitter pre-deposition temperature on the electrical characteristics of two types of double-diffused polysilicon emitter bipolar transistors, one with an ultra thin oxide grown intentionally at the polysilicon/single-crystal silicon interface and the other without, have been studied. With an emitter pre-deposition temperature of 900°C, the integrity of the thin interfacial oxide is preserved and it acts as an effective tunnelling barrier to the minority carrier (hole) injection from the base into the emitter. This leads to a current gain improvement of about three times for a transistor with an interfacial oxide over that without. No similar current gain enhancement is observed with an emitter pre-deposition temperature of 950°C because the thin interfacial oxide is damaged during the higher temperature emitter pre-deposition processing. It is also found that the interfacial oxide hinders emitter dopant diffusion from the polysilicon into the underlying single-crystal silicon region.

INTRODUCTION

The introduction of polysilicon into the bipolar transistor technology has opened up new ways of fabricating the device and, more importantly, such devices have superior characteristics compared to conventional transistors. For example, this has led to the realisation of self-aligned devices^{1,2,3} with a consequent improvement in both switching speed and packing density because of the drastic decrease in transistor size and the accompanying parasitic capacitances and resistances. Furthermore, the use of heavily doped polysilicon as a diffusion source of emitters and/or emitter contacts of bipolar transistors has provided an easy means of achieving very shallow junctions with high yields. These high yields result from a reduction in anomalous diffusion effects⁴ and in defect generation^{5,6} associated with the high concentration emitter diffusion⁷, and also from the elimination of contact spiking.

In addition to the advantages mentioned above, improved current gain can be obtained for transistors with polysilicon emitters⁸. Improvements from 3^9 to $30^{10,11}$ times over similarly processed conventional bipolar transistors have been reported. Although polysilicon emitter bipolar transistors have higher current gain, they also have higher emitter resistance compared to conventional transistors¹². This is highly undesirable because a high emitter resistance will limit the current carrying capability of the transistor. More detrimentally, this can decrease the voltage swing and noise margins of logic circuits and can eventually upset the proper switching of the circuits¹³. It has been reported that the current gain improvements and the higher emitter resistance of polysilicon emitter transistors depend strongly on the processing details of the polysilicon emitter, for example, the surface treatment prior to polysilicon deposition⁸ and the dopant species of the polysilicon emitter¹².

In this paper, the authors investigate further the effect of polysilicon emitter processing details on the electrical characteristics of polysilicon emitter bipolar transistors. In particular, the effects of polysilicon emitter pre-deposition temperature in a double-diffused polysilicon emitter bipolar process are studied.

POLYSILICON EMITTER BIPOLAR TRANSISTOR FABRICATION

Figure 1 shows the difference between a conventional bipolar transistor and the two types of polysilicon emitter transistors that have been successfully fabricated in our laboratory (NPN transistors have been depicted). The only difference between the two types of polysilicon emitter transistors is their surface treatment prior to polysilicon deposition. One treatment is aimed at removing all native oxide present at the single-crystal silicon surface within the emitter window [Figure 1(b)] immediately before polysilicon deposition whereas the other is intended to grow a layer of ultra thin oxide, approximately 20 Å thick, at the polysilicon/single-crystal silicon interface [Figure 1(c)]. The first type of polysilicon emitter transistor has been shown to have a current gain enhancement of two to three times over a similar conventional transistor⁹ and the second type, a further improvement of about ten times over the first type⁸.

The fabrication of polysilicon emitter transistors is identical to that of conventional bipolar transistors up to the emitter window definition step. For the former, after the emitter window is opened, the desired surface treatment is carried out followed by the deposition of a layer of polysilicon instead of subjecting the wafer directly to an emitter doping process, as in the case of the latter. The polysilicon layer can be doped or undoped during its deposition stage. If it is undoped, an additional step is then performed to dope the polysilicon heavily with the desired emitter dopant. This step is equivalent to the emitter pre-deposition in a conventional bipolar process. The polysilicon layer is then patterned to remove the unwanted polysilicon and an emitter drive-in follows during which

(a) Conventional transistor

(b) Polysilicon emitter transistor – without interfacial oxide

(c) Polysilicon emitter transistor – with interfacial oxide

Fig. 1 Comparison between conventional and polysilicon emitter bipolar transistors.

the dopants diffuse from the polysilicon into the underlying single-crystal silicon region, thus creating a shallow base-emitter junction in the single-crystal silicon region, as shown in Figures 1(b) and 1(c). The processing is completed by the usual subsequent contact window cut and metallisation steps.

EXPERIMENT

The polysilicon emitter bipolar transistors were fabricated on 2 inch N-type substrate. The base was formed by thermal diffusion using solid boron glass source, with the pre-deposition carried out at a temperature of 850°C. This is followed by a base drive-in at a temperature of 1,000°C in a wet O₂ ambient, in order to diffuse boron atoms further into the substrate as well as to grow an oxide of sufficient thickness required for the subsequent emitter window definition. After the emitter window was opened, the silicon wafers were given either BHF or RCA surface treatment. In the BHF treatment, silicon wafers were dip-etched in buffered hydrofluoric (BHF) acid for 30 seconds and this was intended to remove all native oxide present at the single-crystal silicon surface within the emitter window. However, a residual oxide of about 4 Å has been shown to remain at the surface¹⁴. The RCA treatment involved boiling the wafers in two cleaning solutions -- H₂O : NH₄OH : H₂O₂ (5 : 1 : 1) and H₂O : HCl : H₂O₂ (6 : 1 : 1) -- in that sequence, for 10 minutes each. This method was expected to produce an ultra thin oxide of approximately 14 Å¹⁴. Details of the two surface treatments, BHF and RCA, and their expected oxide thicknesses are summarised in Table 1.

TABLE 1
SURFACE TREATMENT DETAILS AND
EXPECTED OXIDE THICKNESSES

Surface Treatment	Description	Expected Oxide Thickness / Å
BHF	Dip-etch in buffered hydrofluoric (BHF) acid for 30 seconds	~ 4
RCA	Boil in 1) H ₂ O : NH ₄ OH : H ₂ O ₂ (5 : 1 : 1) followed by 2) H ₂ O : HCl : H ₂ O ₂ (6 : 1 : 1) for 10 minutes each	~ 14

Following the surface treatment, a layer of undoped polysilicon, approximately 3,000 Å, was deposited onto the silicon wafers using a Low Pressure Chemical Vapour Deposition (LPCVD) reactor at a temperature of 600°C and a pressure of 0.6 Torr. After that, the polysilicon layer was pre-doped with phosphorus by thermal diffusion in a N₂ - O₂ - POCl₃ ambient for 10 minutes at a temperature of either 900°C or 950°C. The polysilicon layer was then patterned and a layer of 0.25 µm LPCVD silicon oxide was deposited onto the wafers. This oxide layer was necessary to prevent the out-diffusion of emitter dopants from the polysilicon during the subsequent emitter drive-in and also for the contact window cut. The emitter drive-in was carried out in a N₂ ambient at a temperature of 900°C for 30 minutes. The contact windows were then cut for metallisation, and finally metal tracks were defined and sintered in a H₂/N₂ ambient at a temperature of 400°C for 15 minutes.

A total of four wafers were used in device fabrication and the differences in their emitter processing details are summarised in Table 2.

TABLE 2
EMITTER PROCESSING DETAILS OF POLYSILICON
EMITTER BIPOLAR TRANSISTORS

Wafer	Surface Treatment	Emitter Pre-Deposition Temperature / °C
1	RCA	950
2	RCA	900
3	BHF	950
4	BHF	900

RESULTS AND DISCUSSION

A. Sheet Resistance Versus Emitter Pre-Deposition Temperature

Sheet resistances of the various diffusion regions defined in Figure 2 were measured by means of the Van der Pauw technique¹⁵ and the results are shown in Table 3. These Van der Pauw structures were fabricated on the same wafer as the transistors. In Table 3, the intrinsic base sheet resistance R_{sbi} of wafer 3 is not provided because the meter readings were not stable during measurements. This was most probably due to bad contact on the wafer. From Table 3, it is observed that the extrinsic base sheet resistances R_{sbx} of all four wafers are the same. This is not unexpected as R_{sbx} is not affected by the surface treatment prior to polysilicon deposition and therefore the only difference in processing is the emitter pre-deposition temperature : 950°C for wafers 1 and 3, and 900°C for wafers 2 and 4. The emitter pre-deposition, however, was carried out for only 10 minutes and hence will not affect the extrinsic base dopant profile significantly. This was verified by means of SUPREME¹⁶ simulations, which predict base depths of 0.807 μm and 0.812 μm for wafers having emitter pre-deposition temperatures of 900°C and 950°C respectively.

TABLE 3
SHEET RESISTANCES AND CURRENT GAIN OF
POLYSILICON EMITTER BIPOLAR TRANSISTORS

Wafer	Sheet Resistance / / square				Maximum Current Gain
	Intrinsic Base R_{sbi}	Extrinsic Base R_{sbx}	Poly. on Oxide R_{spi}	Poly. on Silicon R_{sp2}	
1	13,300	562	54.4	12.7	900
2	1,750	562	104.4	91.5	225
3	----	562	54.4	11.3	1,200
4	3,700	562	92.0	52.1	80

Fig. 2 The various diffusion regions

Comparing the intrinsic base sheet resistance R_{sbi} of wafers 2 and 4, which have an emitter pre-deposition temperature of 900 °C, the RCA treated wafer (wafer 2) is found to have a much lower R_{sbi} than the BHF treated wafer – approximately half – although R_{sbx} is the same for both, as shown in Table 3. The only difference in processing between wafers 2 and 4 is the surface treatment prior to polysilicon deposition, hence this must be mainly responsible for the marked difference in their R_{sbi} . The RCA treatment was used to intentionally grow an ultra thin oxide of approximately 14 Å¹⁴ at the polysilicon/single-crystal silicon interface within the emitter window whereas the BHF treatment was used to remove all native oxide at the same interface. Therefore, it can be deduced that the interfacial oxide layer grown by the RCA treatment has hindered emitter dopant diffusion from the polysilicon into the single-crystal silicon region, thereby resulting in a lower R_{sbi} for the RCA-treated wafer compared to the BHF-treated wafer. This deduction is corroborated by comparing the sheet resistance of polysilicon layer on oxide R_{sp1} with that of the polysilicon layer on single-crystal silicon R_{sp2} . The former is the sheet resistance of the polysilicon layer only whereas the latter includes the single-crystal silicon region underneath the polysilicon layer, as demonstrated in Figure 2. It is observed in Table 3 that although R_{sp1} is about the same for wafers 2 and 4, R_{sp2} is much higher for the RCA-treated wafer than for the BHF-treated wafer. In addition, it is seen that R_{sp2} is not much lower than R_{sp1} for wafer 2 thus indicating that penetration of emitter dopants from the polysilicon layer into the underlying single-crystal silicon layer is not very significant for the RCA-treated wafer. For wafer 4, R_{sp2} is much less than R_{sp1} , hence the penetration is deeper for the BHF-treated wafer.

An examination of the results of wafers 1 and 3 in Table 3 reveals that the situation is very different if the emitter pre-deposition is carried out at a higher temperature, i.e. 950°C. A comparison of R_{sp1} and R_{sp2} of wafers 1 and 3 shows that the emitter dopant penetration into the single-crystal silicon is not affected dramatically by the interfacial oxide layer grown by the RCA treatment, as the two polysilicon layer sheet resistances are comparable for both wafers: R_{sp2} of wafer 1 (RCA device) is only slightly higher than that of wafer 3 (BHF device). Jorgensen et al.¹⁴ has shown that the RCA thin interfacial oxide will break up and the polysilicon/single-crystal silicon interface will undergo structural changes if any processing subsequent to the thin oxide layer growth is performed at a temperature beyond 900°C. Hence, it could be said that the RCA thin interfacial oxide layer has most probably deteriorated during the 950°C emitter pre-deposition step thus providing little or no hindrance to emitter dopant penetration. Following the discussion in this paragraph, one can expect that the intrinsic base sheet resistance R_{sbi} of wafer 3 should be approximately equal to or not much less than that of wafer 1.

Looking at the intrinsic base sheet resistance R_{sbi} column of Table 3, it is obvious that the higher 950°C emitter pre-deposition temperature has 'pushed' the emitter deeper into the single-crystal silicon compared to the 900°C emitter pre-deposition temperature as R_{sbi} is much higher for wafer 1 than for wafer 2. This is also manifested by the much lower R_{sp2} for wafers 1 and 3 than for wafers 2 and 4.

B. Device D.C. Characteristics

The d.c. characterisation of the polysilicon emitter bipolar transistors fabricated was carried out using a Hewlett/Packard Semiconductor Parameter Analyser HP 4145B. The base and collector currents, I_B and I_C , of the transistors were measured as a function of the transistor base-emitter junction voltage V_{BE} and the results are plotted in Figure 3. The plot of $\ln(I_B)$ and $\ln(I_C)$ versus V_{BE} for $V_{BC} = 0$ is known as a Gummel plot. Measurements were done on devices with an emitter area of $100 \times 100 \mu\text{m}^2$.

From Figure 3, it is observed that I_B of wafer 2 is more than ten times lower than that of wafer 4 in the low current range. This must be caused by the surface treatment prior to polysilicon deposition since that is the only difference in processing between the two wafers. The RCA treatment grows an approximately 14 Å thin oxide layer at the polysilicon/single-crystal silicon interface. Such a thin interfacial oxide layer has been shown to act as a tunnelling barrier to carriers and can suppress the injection of minority carriers (holes) from the base into the emitter¹⁰. It is seen in the last section that the thin interfacial oxide layer grown by the RCA treatment is not damaged at an emitter pre-deposition temperature of 900°C. Consequently, it can be said that the RCA thin interfacial oxide layer

Fig. 3 The I-V characteristics of polysilicon emitter bipolar transistors.

of wafer 2 has acted as an effective tunnelling suppressor to the injection of minority carriers (holes) from the base into the emitter and is therefore responsible for the much smaller I_B in the RCA device compared to the BHF device.

If the base Gummel number, i.e. the effective number of free carriers in the base, of transistors on wafers 2 and 4 are identical, the transistor current gain of the devices on wafer 2 would be more than ten times higher than that of wafer 4, i.e. due to the difference in I_B , since then the collector current I_C (which is inversely proportional to base Gummel number) would be the same for both transistors. However, such a dramatic enhancement in current gain is not realised because the RCA interfacial oxide layer also acts as a hindrance to emitter dopant diffusion from the polysilicon layer into the underlying single-crystal silicon region, as discussed in the last section. Consequently, the base Gummel number is higher (or equivalently the intrinsic base sheet resistance R_{sbi} is lower) for the RCA device than for the BHF device and this leads to a lower I_C for the former as depicted in Figure 3. Taking this into consideration, the current gain enhancement due to the presence of an intentionally grown interfacial oxide layer is therefore much less than the expected ten times. The current gain of wafer 2 is only approximately 3 times that of wafer 4, as shown in Table 3.

Going back to Figure 3, it is observed that for wafers 1 and 3, the results are very different from those of wafers 2 and 4 -- the RCA device has a higher, instead of lower, I_B than the BHF device. From previous discussion, we know that the RCA interfacial oxide layer has deteriorated during the 950°C emitter pre-deposition step and therefore will no longer be a very effective tunnelling layer that will suppress the minority carrier (hole) injection from the base into the emitter significantly. This in turn leads to a drastic decrease in the transistor current gain of the RCA device of wafer 1 compared to a similar transistor with an intact interfacial oxide layer¹⁴. The higher I_B of the RCA device compared to that of the BHF device, which is not expected, can be explained as follows. The intentionally grown RCA interfacial oxide is not deteriorated at the beginning of the emitter pre-deposition step and therefore acts as an effective barrier to emitter dopant diffusion at the start of the process and less so as the pre-deposition proceeds. This results in a shallower penetration of emitter dopants into the single-crystal silicon region and therefore a lower effective emitter Gummel number and a higher I_B for the RCA device over the BHF device.

The difference in I_C for wafers 1 and 3 is similar to that for wafers 2 and 4, i.e. higher I_C for the BHF device. However, the difference is much less in the former. This is expected as the RCA oxide is destroyed during the higher temperature emitter pre-deposition step for wafer 1, and hence it is not as effective as in wafer 2 as an emitter dopant diffusion barrier. The overall effect of a 950°C emitter pre-deposition temperature and the consequent deterioration of the RCA

thin oxide is a lower transistor current gain for the RCA device (wafer 1) than for the BHF device (wafer 3), as shown in Table 3. This is opposite to that of devices having a lower emitter pre-deposition temperature of 900°C.

Comparing wafers having different emitter pre-deposition temperature, one can clearly see that the higher temperature has led to a higher emitter dopant concentration, as implied by the higher I_B for wafer 4 than for wafer 3. For the RCA devices, because of the presence of the tunnelling oxide, the magnitude of I_B is not a direct indication of the emitter dopant concentration¹⁰. In addition to providing higher emitter dopant concentration, the higher emitter pre-deposition temperature also pushed the emitter deeper into the base region, therefore leading to a much higher I_C (or lower base Gummel number) for wafers 1 and 3 than for wafers 2 and 4, as shown in Figure 3.

The rather severe bending in I_B and I_C at high currents shown in Figure 3 is caused by the transistor ohmic base and emitter resistances and/or high current injection effects. This indicates that the emitter resistance of the polysilicon emitter bipolar transistors fabricated could be much higher than that of conventional transistors, as has been reported^{12,13}.

CONCLUSION

Two types of polysilicon emitter bipolar transistors, one with an intentionally grown thin oxide at the polysilicon/single-crystal silicon interface and the other without, have been successfully fabricated using a double-diffused scheme. The effects of emitter pre-deposition temperature on the device electrical characteristics have been studied. At a temperature of 900°C, the intentionally grown thin oxide layer at the polysilicon/single-crystal silicon interface is preserved and acts as an effective base current suppressor, thus leading to an enhancement in the transistor current gain. The RCA interfacial oxide layer is believed to deteriorate and the polysilicon/single-crystal silicon interface to undergo structural changes at an emitter pre-deposition temperature of 950°C and this results in no current gain improvement in the RCA device over the BHF device. The RCA interfacial oxide layer has also been shown to hinder emitter dopant diffusion from the polysilicon into the single-crystal silicon region and the amount of hindrance is dependent on the heat treatment subsequent to the interfacial oxide layer growth. In summary, it is concluded that the electrical characteristics of polysilicon emitter bipolar transistor is sensitive to the emitter pre-deposition temperature because this can affect the integrity of the polysilicon/single-crystal silicon interface.

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